Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An integrated module, comprising:

an external access terminal;

a memory including memory cells and redundant memory cells for storing code and data, said redundant memory cells being combined to form redundant row lines or redundant column lines;

a microcontroller connected to said external access terminal and to said memory, said microcontroller controlling an access to said memory and a data transfer through said external access terminal during normal operation, said microcontroller controlling a performance of a test sequence for functional testing said memory in a test operation of the module; and

the microcontroller including a defect data memory for storing addresses of the memory cells of said memory which have been detected as defective to calculate a repair solution to replace regular lines having defective memory cells with the

redundant row lines or redundant column lines, said addresses being generated during the functional testing, said addresses being stored in said defect data memory under control of said microcontroller, said addresses further being read out under control of said microcontroller, to outside of the integrated module~~, and used to calculate a repair solution to replace regular lines having defective memory cells with the redundant row lines or redundant column lines~~.

Claim 2 (original): The integrated module according to claim 1, further comprising a command memory for storing an externally supplied command sequence and on a basis of the command sequence said microcontroller controls a carrying out of the test sequence.

Claim 3 (original): The integrated module according to claim 1, wherein said defect data memory is part of said microcontroller.

Claim 4 (original): The integrated module according to claim 2, wherein said command memory is part of said microcontroller.

Claim 5 (currently amended): A method for functionally checking a memory including memory cells and redundant memory cells of an integrated module, which comprises the steps of:

reading-in a command sequence externally before beginning a test operation, and on a basis of the command sequence a microcontroller controls a carrying out of a test sequence;

executing the command sequence for carrying out the test sequence by the microcontroller;

storing addresses of the memory cells of the memory which have been detected as defective during the functional testing in a defect data memory in the microcontroller, said addresses being stored in said defect data memory under control of said microcontroller for use in calculating a repair solution to replace regular lines having defective memory cells with the redundant row lines or redundant column lines;

reading-out the addresses of the memory cells of the memory which have been detected as defective during functional testing stored in the defect data memory, under the control of the microcontroller, to outside the integrated module for further evaluation; and

using the read-out addresses of the defective memory cells to calculate a repair solution that replaces regular lines having defective memory cells with redundant row lines or redundant column lines formed by redundant memory cells.

Claim 6 (previously presented): The method according to claim 5, which further comprises:

making a jump to a start address in an internal command memory after the command sequence is read-in at the beginning of the test operation;

executing the command sequence under the control of the microcontroller proceeding from the start address; and

storing the addresses of the memory cells of the memory which have been detected as defective during functional testing generated in the defect data memory under the control of the microcontroller.

Claim 7 (previously presented): The integrated module according to claim 1, wherein said defect data memory and said command memory are part of a dual-port RAM.

Claim 8 (previously presented): The integrated module according to claim 1, wherein the microcontroller is embodied as a hard disk controller.